

FIELD OF THE INVENTION AND RELATED ART

~~Isis~~ az

15 In recent years, as picture display apparatus
for computer apparatus, etc., those of the so-called
multiscan-type capable of displaying picture signals
having various frequencies (or resolutions) become
popular. In this regard, picture signals inputted
from the exterior are not always of a prescribed
single format, but even picture signals having an
identical resolution can have different horizontal or
vertical initial or starting points of display on an
entire display picture area or a display panel. This
20 means that the deviation in starting point of display
can lead to a lack of display picture in the case of a
dot matrix-type picture display apparatus wherein a
picture display region corresponds to a number of
display pixels. Accordingly, the picture display
25 apparatus is required to have a means for displaying a
picture at an exact position corresponding to inputted

picture signal.

Figure 5 is a block diagram showing an organization of a conventional picture display apparatus. Referring to Figure 5, the picture display apparatus includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, and a preset data memory 5. Based on the organization, analog video signals Ra, Ga and Ba are converted by the A/D converter 1 into digital signals Rd, Gd and Bd, which are then stored at a picture memory contained within the picture display unit drive circuit 2. The time of writing in the picture memory is controlled by the display control circuit 4. At the picture display unit drive circuit 2, picture data processing for producing signals R, G and B suitable for the picture display unit 3 is effected, and drive timing pulses (horizontal synchronizing pulses H, vertical synchronizing pulses V and pixel clock signals CK) are generated. In this organization, the display position adjustment is performed by storing preset picture position data based on expected input signal formats in the preset data memory 5, and judging the inputted signal format by the display control circuit 4 to set the picture display position to the preset value. Accordingly, an accurate position adjustment is impossible for inputted signals other than expected

input signals, so that there is provided an adjustment means for allowing an operator to effect a manual position adjustment.

Figure 6 is a block diagram of another
5 example of conventional picture display apparatus, which includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, and a picture position detection circuit 6'. Based on this organization, the
10 picture position detection circuit 6' is supplied with converted digital video signals Rd, Gd and Bd, a horizontal synchronizing signal H_{SYNC}, a vertical synchronizing signal V_{SYNC} and a dot clock signal DCK. By detecting positions of digital video signals Rd, Gd
15 and Bd corresponding to the horizontal synchronizing signal H_{SYNC} and the vertical synchronizing signal V_{SYNC} by the position detection circuit 6' and based on the results thereof, the display control circuit 4 controls the timing for writing the digital video
20 signals Rd, Gd and Bd in a picture memory contained in the picture display unit control circuit 2, thereby automatically adjusting the picture display position on the display unit (Japanese Laid-Open Patent Application (JP-A) 7-44125 and JP-A 10-63234).

Sub 23
The picture display apparatus of Figure 5
23
unnecessitates a manual adjustment for signal formats for which preset values have been set, but for signals

of other formats, the operator is required to effect a troublesome manual adjustment of horizontal and vertical positions while observing a picture displayed on the display unit and the adjustment is also

5 difficult. On the other hand, the picture display apparatus of Figure 6 allows an automatic positional alignment but in view of higher resolution and higher input signal frequency adopted in recent years, the operation speed of the picture position detection
10 circuit 6' is increased correspondingly to result in an increased current flow and a higher-speed expensive circuit device for realizing the picture position detection circuit 6', thus incurring an increased production and running cost. Particularly, in the
15 case of effecting the picture position adjustment dot by dot, a substantial time is required for display position adjustment to cause a delay in commencement of display.

20 SUMMARY OF THE INVENTION

In view of the above-mentioned problem of the prior art, a principal object of the present invention is to provide a picture display apparatus equipped with means for detection and automatic adjustment of
25 display position at a reduced current consumption and at a low cost in a dot matrix-type picture display apparatus.

According to the present invention, there is provided a picture display apparatus for displaying a picture in response to inputted picture signals of arbitrary format, comprising:

- 5 a picture display apparatus having an arranged matrix of dots for picture display,
- picture display unit drive means for converting inputted picture signals into display picture signals adapted for display on the picture
- 10 display unit and generating drive timing signals for driving the picture display unit,
- display position detection means for detecting a picture display position on the picture display unit based on the display picture signals and
- 15 the drive timing signals, and
- display position control means for controlling admission of the inputted picture signals to the picture display unit drive means based on the detected display position data from the display
- 20 position detection means.

 These and other objects, features and advantages of the present invention will become more apparent upon a consideration of the following description of the preferred embodiments of the

25 present invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram of an embodiment of the picture display apparatus according to the invention.

5 ~~Figure 2 is a time chart for illustrating an example of display position relative to a horizontal synchronizing signal.~~

10 ~~Figure 3 is a time chart for illustrating an example of display position relative to a vertical synchronizing signal.~~

Figure 4 is a flow chart illustrating a system flow of display position adjustment for the apparatus of Figure 1.

15 Figures 5 and 6 are respectively a block diagram of a conventional picture display apparatus including a picture display adjustment system.

Figure 7 is a time chart illustrating an example of outputted picture data.

20 DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Figure 1 showing an embodiment of the picture display apparatus according to the present invention, the picture display apparatus includes a picture display unit 3, an A/D conversion circuit 1 for converting inputted analog picture signals Ra, Ga and Ba into digital signals Rd, Gd and Bd, a picture display unit drive circuit 2 for

converting the digitally converted video signals Rd, Gd and Bd into display picture signals R, G and B suitable for displaying on the picture display unit 3 and generating drive timing signals for driving the picture display unit 3, a display picture detection circuit 6 for receiving the digital picture signals R, G and B, a horizontal synchronizing signal H, a vertical synchronizing signal V and pixel clock signals CK for the picture display unit 3 prepared by the picture display unit drive circuit 2 to detect horizontally initial and final points and vertically initial and final points for a display picture on the picture display unit 3, a display control circuit 4, and a preset data memory 5, wherein the timing for writing the digital signals Rd, Gd and Bd into a picture memory 2m contained in the picture display unit drive circuit 2 is controlled based on the display position detection circuit 6, thereby automatically adjusting a display picture position.

Further, by disposing the display position detection circuit 6 at a later stage than the picture display unit drive circuit 2, the operation speed of the display position detection circuit 6 is restricted within the drive speed of the picture display unit 3, whereby the detection circuit 6 can be operated at a suppressed current consumption and does not require a high-speed device incurring an increased apparatus

cost.

Further, by adopting a system sequence or flow of effecting an automatic picture position adjustment immediately before displaying a first picture in the picture display apparatus, it becomes possible to realize a system whereby an operator is unconscious of positional deviation of a display picture.

Hereinbelow, the operation of the embodiment will be described in further detail.

As mentioned above while referring to Figure 1, the picture display apparatus includes an A/D converter 1, a picture display unit drive circuit 2, a picture display unit 3, a display control circuit 4, a preset data memory 5 and a display position detection circuit 6. Inputted analog video signals Ra, Ga and Ba are converted into digital signals Rd, Gd and Bd by the A/D converter 1 based on a dot clock signal DCK, and the digital signals are inputted to the picture display unit drive circuit 2.

The picture display unit drive circuit 2 includes a picture memory 2m, and the converted digital video signals Rd, Gd and Bd are once stored in the picture memory 2m based on the dot clock signal DCK, and then read out based on a clock signal having a frequency different from that of the dot clock signal DCK to be processed so as to provide display

picture signals suitable for display on the picture display unit 3. According to the system organization, the timing of readout from the picture memory 2m is fixed, so that the picture display position on the picture display unit 3 is determined by the time when the digital video signals Rd, Gd and Bd are written in the picture memory based on the dot clock signal DCK. More specifically, if the writing in the memory 2m is effected at a horizontally early time, the display picture signal is outputted from the picture display unit drive circuit 2 at an early time to provide a picture display position shifted to a right side on the picture display unit 3. On the other hand, if the writing in the picture memory 2m is effected at a horizontally late time, the display picture outputted from the picture display unit drive circuit 2 at a later time to provide a picture display position shifted to a left side on the picture display unit 3. Similarly, the writing in the picture memory 2m at a vertically early time results in a picture display position shifted to a lower side and the writing in the memory 2m at a vertically late time results in a picture display position shifted to an upper side on the picture display unit 3.

The picture display unit drive circuit 2 also generates drive timing pulses (i.e., horizontal synchronizing pulses H, vertical synchronizing pulses

V and pixel clock signals CK) for the picture display unit 3. The video signals R, G and B prepared by processing in the picture display unit drive circuit 2 are inputted to the picture display unit 3 along with these timing pulses to display a picture on the picture display unit 3.

The timing of writing the digital video signals Rd, Gd and Bd in the picture memory is controlled by the display control circuit 4. The video signals R, G and B, the horizontal synchronizing signal H, the vertical synchronizing signal V and the pixel clock signal CK outputted from the picture display unit drive circuit 2, are also inputted to the display position detection circuit 6. The display position detection circuit 6 includes a counter for counting pixel clock pulses CK from a point of rise of the horizontal synchronizing signal H to detect a time HFC based on the number of clock pulses CK corresponding to a point of commencement of inputted video signals R, G, B and a time HRC based on the number of clock pulses CK corresponding to a point of termination (or absence) of the inputted video signals with respect to the horizontal position as shown in Figure 2. Further, the display position detection circuit 6 also includes a counter for counting the horizontal synchronizing pulses H from a point of rise of the vertical synchronizing signal V to detect a

time VFC based on the number of the horizontal
synchronizing pulses H corresponding to a point of
commencement of the video signals and a time VRC based
on the number of horizontal synchronizing pulses H
5 corresponding to a point of termination (or absence)
of the inputted video signals. The position data HFC,
HRC, VFC and VRC detected by the display position
detection circuit 6 are inputted to the display
control circuit 4, where differences of these values
10 from set picture signal outputting timing values are
determined. Based on the differences, the display
control circuit 4 controls the timing of writing newly
inputted digital signals Rd, Gd and Bd in the picture
memory 2m contained in the picture display drive
15 circuit 2. For example, at VIDEO, Figure 7 shows a
case where a small difference on the order of several
dots is present between the actual memory writing
timing and the set memory writing timing, accordingly
between the detected horizontal initial display
20 position data HFC and a set horizontal initial display
position data Phf. Based on the difference between
HFC and Phf, the display control circuit 4 controls
the timing of writing newly inputted digital data Rd,
Gd and Bd in the picture memory 2m in the picture
25 display unit drive circuit 2 according to an
adjustment sequence illustrated in a flow chart of
Figure 4 as will be described hereinafter.

On the other hand, in case where there is a large difference between the actual memory writing time and the set memory writing time, e.g., a difference of more than 304 dots exceeding a blanking period for inputted picture signals in an assumed case including totally 1328 dots within an interval between subsequent horizontal synchronizing signals and 1024 display dots, the video signal output from the picture display unit drive circuit 2 assumes a form as shown at VIDEO' in Figure 7. In Figure 7, Phr denotes a horizontal picture data output termination, whereas the writing time into the picture memory is deviated by more than on blanking period, the picture data outputted from the picture display unit drive circuit 2 beginning from time Phf and ending with time Phr is caused to include a blanking period therein. As a result, while the display position is actually remarkably deviated, the display position data HFC and HRC detected by the display position detection circuit 6 happen to be identical to set timing data of Phf and Phr, thus obstructing an accurate adjustment.

For obviating the above difficulty, a minimum degree within a necessary extent of preset data (e.g., ideal pixel memory writing timing data for each of representative resolution formats such as VGA, SVGA and XGA) are stored in the preset data memory 5, and one of such preset format data is stored in advance in

the picture display unit drive circuit 2 after judging the inputted signal format in the display control circuit 4, thereby by obviating the occurrence of an extreme positional deviation as shown at VIDEO' in Figure 7. After obviating such an extreme deviation, a minor degree of deviation as shown at VIDEO in Figure 7 is removed by controlling the timing for writing digital data in the pixel memory in the circuit 2 according to the adjustment flow of Figure 4.

Incidentally, in the above embodiment, picture signals in three types of R, G and B are inputted in the display position detection circuit 6, but it is possible to adopt a simple scheme of introducing only one type among R, G and B signals.

Figure 4 is a flowchart illustrating a display position adjustment sequence adopted in an embodiment of the picture display apparatus according to the present invention.

Referring to Figure 4, as a first step S1 of display position adjustment, horizontal and vertical display position data HFC, HRC, VFC and VRC are detected by the display position detection circuit 6. Then, at step S2, the set horizontal output commencement time Phf and vertical output commencement time Pvf from the picture display unit drive circuit 2 are compared with actual horizontal output

5

15

$$Mv = Mvs + [VFC - Pvf] \quad \dots (2),$$

20

25

INS
aid

position detection circuit 6. As a result of comparison, if the compared results are unequal, this means that the timing of writing digital data in the picture memory 2m is slower (i.e., too late; on the other, in case where the time is faster, no positional deviation in display termination position is recognized as the data is present at the time after reading out of the memory and prescribed processing of read data), and an operator at step S5 of adjusting the horizontal writing time Mh and a vertical writing time Mr respectively according to the following formulae:

$$Mh = Mhs - [Phr-HRC] \quad \dots(3)$$

$$Mv = Mvs - [Pvr-VRC] \quad \dots(4).$$

If the comparison results at step S4 are equal, an operation at step S6 is performed.

At step S6, the display positions are so that:

$$Mh = Mhs \quad \dots(5)$$

$$Mv = Mvs \quad \dots(6).$$

Then, the display position adjustment is completed.

On the other hand, it is also possible to place a step S7 where the initial values Mhs and Mvs are renewed according to the following formulae (7) and (8) based on the values of Mh and Mv according to the above formulae (3) and (4):

$$Mhs = Mh \quad \dots(7)$$

Mvs = Mv ... (8).

By effecting the above display position adjustment sequence just before a first picture display after turning on power supply to the picture display apparatus or just before display a first picture according to a new picture signal format after converting the previous picture signal format to the new picture signal format, it is possible to realize a display system wherein an operator is not conscious of a display picture positional deviation.

As described above, according to the present invention, by detecting a picture display position from picture data outputted from a picture display unit drive circuit, it becomes possible to effect an accurate display position detection on a picture display unit. Further, by using the result as a basis for controlling the timing for writing inputted video signals in a picture memory contained in the picture display unit drive circuit, it is possible to realize a good picture free from a partial lack of the picture.

Further, by disposing the display position detection unit in a later stage than the picture display unit drive circuit, i.e., in a drive environment of the picture display unit, the operation speed of the display position detection circuit can be lowered, thereby allowing an operation at a reduced

current consumption and adoption of a low-speed device for the circuit, leading to a reduced production cost.

5

10

15

20

25